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Signature

John D. Lanza

Please Print Name of Person Signing

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Thomas M. Olson

Application number: 09/550,108

Filed: April 14, 2000

For: METHOD AND APPARATUS FOR PERSISTENT VOLATILE COMPUTER MEMORY

Attorney Docket No.: SRT-002

Group Art Unit: 2186

Examiner: Pierre-Michel Bataille

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

As indicated in the Notice of Appeal filed on March 19, 2004, Appellant hereby appeals the final decision of the Examiner in the above-identified application rejecting the subject matter of the pending claims. A Petition for a One-Month Extension of Time Under 37 CFR 1.136(a) is enclosed. In view of the reasons set forth below, Appellant respectfully requests the Board of Patent Appeals and Interferences to reverse the Examiner's final rejection of the claimed subject matter.

1. Real Party in Interest

The real party in interest in the above-identified application is Stratus Technologies Bermuda Ltd.

2. Related Appeals and Interferences

No other appeals or interferences are known to Appellant, the Appellant's legal representative, or assignee that will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

3. Status of Claims

Claims 1-23 are pending in the application.

Claims 1-23 and are on appeal and are set forth in Appendix A.

4. Status of Amendments

No amendment was filed subsequent to final rejection mailed on December 22, 2003 (Paper No. 13).

5. Summary of Invention

As defined by the claims on appeal, Appellant's invention relates to a computer operating under control of an operating system. See, e.g., Specification, at page 6, line 24 through page 7, line 16, and reference character 10' in Fig. 2. In the computer, there is a volatile memory that is partitioned into at least two memory regions. See, e.g., Specification, at page 6, line 24 through

page 7, line 16, and reference character 20 in Fig. 2. A first region is a contiguous, non-persistent memory region that is directly accessible by the operating system and initialized during a boot cycle. See, e.g., Specification, at page 6, line 24 through page 7, line 16, and reference character 40 in Fig. 2. A second memory region is a contiguous, persistent memory region that is not directly accessible by the operating system and not initialized during a boot cycle. See, e.g., Specification, at page 6, line 24 – page 7, line 16 and reference character 42 in Fig. 2. An intermediary program may be provided for communicating with the operating system and the second memory region to enable the operating system to address the second memory region. See, e.g., Specification, at page 7, line 17 through page 8, line 24, and reference character 28' in Fig. 3.

6. Statement of Issues Presented for Review

Appellant presents the following issues for review:

(1) Whether claims 1-5, 11, 13-14, 18-21 and 23 are obvious over United States Patent No. 5,694,583 to Williams *et al.* ("Williams") in view of United States Patent No. 6,636,963 to Stein *et al.* ("Stein");

(2) Whether claims 6-9 are obvious over Williams in view of Stein, and further in view of United States Patent No. 5,383,161 to Sanemitsu ("Sanemitsu");

(3) Whether claims 10, 15 and 22 are obvious over Williams in view of Stein, and further in view of United States Patent No. 5,799,324 to McNutt *et al.* ("McNutt");

(4) Whether claims 16-17 are obvious over Williams in view of Stein, and further in view of United States Patent No. 5,875,465 to Kilpatrick *et al.* ("Kilpatrick"); and

(5) Whether claim 12 is properly objected to as being dependent upon a rejected base claim although claim 11, which claim 12 depends from, recites patentable subject matter.

7. Groups of Claims

All the claims on appeal, i.e., claims 1-23 do not stand or fall together.

Claims 1-5, 11, 13, 14, 18-21 and 23 stand or fall together.

Claim 12 stands or falls alone.

Claims 6-9 stand or fall together.

Claims 10, 15 and 22 stand or fall together.

Claims 16 and 17 stand or fall together.

Claim 23 stands or falls alone.

8. Arguments

Appellant believes that the following arguments address each of the issues presented for appeal.

8.1 Claims 1-5, 11, 13-14, 18-21 and 23 are not obvious over Williams in view of Stein because there is no motivation to combine those references and, even when combined, they fail to teach or suggest all the limitations recited by the claims.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable

expectation of success must both be found in the prior art, not in Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP §2142.

The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (BPAI 1985); MPEP §2142.

8.1.1. <u>There is no motivation to combine the teachings of Williams and Stein</u>

Claims 1-5, 11, 13-14, 18-21 and 23 are rejected as obvious over Williams in view of Stein. Appellant respectfully submits that there is no suggestion or motivation, either in the cited references or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of these references because the proposed combination would render the prior art inventions unsatisfactory for their intended purpose. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

Williams describes a computer including a bootable CD-ROM that is capable of emulating several media types, such as a hard drive, a floppy drive, etc. Williams teaches a warm boot process that the computer executes when it desires the CD-ROM to emulate a different media. The warm boot process is <u>required</u> for DOS to recognize the new mode the CD-ROM emulates (<u>See</u> Williams, Abstract).

Stein describes a critical-care, microprocessor-based medical system that is able to transition to a target state quickly. Stein teaches that the microprocessor-based system is capable of transitioning from a powered down condition to an operational state without going through a

time-consuming boot process. (See Stein, Abstract). Thus, Stein teaches a system that avoids booting.

The systems described by Stein and the systems described by Williams cannot be combined because Stein systems avoid booting while Williams systems require booting. If Stein systems are modified to boot, patient care is compromised. If Williams systems are modified to avoid booting, the system will never recognize the new CD-ROM emulation mode. Appellant, therefore, respectfully submits that there is no suggestion or motivation, either in the cited references or in the knowledge generally available to one of ordinary skill in the art, to combine reference teachings. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness and the rejection of claims 1-5, 11, 13-14, 18-21 and 23 under 35 U.S.C. §103 should be reversed.

8.1.2. Williams and Stein fail to teach or suggest all of the claim limitations

Claims 1-5, 11, 13-14, 18-21 and 23 are rejected as obvious over Williams in view of Stein. Appellant argues above why there is no motivation to combine Williams and Stein. Even if combined, however, Williams and Stein fail to teach or suggest all the claim limitations of the claimed invention.

The claimed invention recites, at least in part, a computer system having a volatile memory partitioned into a first, contiguous, non-persistent region and a second, contiguous, persistent memory. The non-persistent region of volatile memory may be directly written to by the operating system and is initialized when the computer is booted. The persistent region of volatile memory is not directly written to by the operating system and is not initialized when the computer is booted.

The Examiner admits in the Final Office Action that Williams does not teach or suggest that a portion of volatile memory is not directly written to by the operating system. Stein is cited to compensate for this deficiency.

However, the Examiner does not identify teachings in Stein that describe a persistent region of a volatile memory that is not directly written to by the operating system. Instead, the Examiner merely concludes that it would have been obvious to provide a portion of volatile memory not directly written by the operating system while another portion is accessible because it would be "inherently" advantageous to first load system information upon booting and, if compatible with registered information of the operating system, make other peripheral devices accessible to the operating system.

While official notice may be relied on in limited circumstances, these circumstances should be rare when an application is under final rejection. MPEP §2144.03. Official notice without documentary evidence to support an examiner's conclusion is permissible only in some circumstances where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known. Any facts in official notice should be of notorious character and serve only to "fill in the gaps" in an insubstantial manner which might exist in the evidentiary showing made by the examiner to support a particular ground for rejection. *In re Zurko*, 258 F.3d 1379 (Fed. Cir. 2001). It is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based. *Id.* at 1385.

Here, the matters of which the Examiner takes "official notice" are not insubstantial. Here, the Examiner takes "official notice" of the very crux of the invention, which is improper. Therefore, it is Appellant's position that the Examiner has failed to establish a *prima facie* case

of obviousness because Williams and Stein fail to teach or suggest a volatile memory partitioned into a first, contiguous, non-persistent region and a second, contiguous, persistent memory. Accordingly, Applicant respectfully submits that the rejection of claims 1-5, 11, 13-14, 18-21 and 23 under 35 U.S.C. §103 should be reversed.

8.2. Claims 6-9 are not obvious over Williams in view of Stein, and further in view of Sanemitsu because those references, even when combined, fail to teach or suggest all the limitations recited by the claims.

Claims 6-9 are rejected as obvious over Williams in view of Stein, and further in view of Sanemitsu. Claims 6-9 depend from independent claim 1 and incorporate the patentable features of claim 1. The arguments presented above with respect to the rejection of claim 1 apply with equal force here and are reiterated as if set forth in full.

Appellant respectfully submits that claims 6-9 are not obvious over Williams, Stein and Sanemitsu because those references, even if combined, fail to teach or suggest all the claim limitations of the claimed invention and, therefore, fail to make a *prima facie* case of obviousness.

Appellant submits that Sanemitsu also fails to teach or suggest the persistent region of volatile memory that is not directly written to by the operating system, as recited in the claimed invention. Sanemitsu is directed to an integrated circuit card that prevents easy rewriting of information stored in the card. (See Sanemitsu, col. 2, lines 14-17). Sanemitsu does not teach or suggest a computer having a volatile memory partitioned into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized.

Williams, Stein and Sanemitsu therefore fail to teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized. Accordingly, Appellant respectfully submits that the combination of Williams, Stein and Sanemitsu does not teach or suggest the invention recited by independent claim 1, that claims 6-9 define patentably over the combination of Williams, Stein and Sanemitsu, and that the rejection of those claims under 35 U.S.C. §103 should be reversed.

8.3. Claims 10, 15 and 22 are not obvious over Williams in view of Stein, and further in view of McNutt because those references, even when combined, fail to teach or suggest all the limitations recited by the claims.

Claims 10, 15, and 22 are rejected as obvious over Williams in view of Stein, and further in view of McNutt. Claims 10, 15 and 22 depend from independent claims 1, 13 and 20, and incorporate the patentable features of claims 1, 13 and 20, respectively. The arguments presented above with respect to the rejections of claims 1, 13 and 20 apply with equal force here and are reiterated as if set forth in full.

Appellant respectfully submits that claims 10, 12 and 22 are not obvious over Williams, Stein and McNutt because those references, even if combined, fail to teach or suggest all the claim limitations of the claimed invention and, therefore, fail to make a *prima facie* case of obviousness.

Appellant submits that McNutt also fails to teach or suggest the persistent region of volatile memory that is not directly written to by the operating system, as recited in the claimed invention. McNutt teaches a system and method for management of persistent data in a log-structured disk array in which persistent data is stored to a disk drive. (See McNutt, Abstract).

McNutt does not teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized. Rather, McNutt merely teaches efficient ways to store persistent data to well-known persistent storage.

Williams, Stein and McNutt therefore fail to teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized. Accordingly, Appellant respectfully submits that the combination of Williams, Stein and McNutt does not teach or suggest the invention recited by independent claims 1, 13, and 20, that claims 10, 15, and 22 define patentably over the combination of Williams, Stein and McNutt, and that the rejection of those claims under 35 U.S.C. §103 should be reversed.

8.4. Claims 16 and 17 are not obvious over Williams in view of Stein, and further in view of Kilpatrick because those references, even when combined, fail to teach or suggest all the limitations recited by the claims.

Claims 16-17 are rejected as obvious over Williams in view of Stein, and further in view of Kilpatrick. Claims 16-17 depend from independent claim 15 and incorporate the patentable features of claim 15. The arguments presented above with respect to the rejection of claim 15 apply with equal force here and are reiterated as if set forth in full.

Appellant respectfully submits that claims 16 and 17 are not obvious over Williams, Stein and Kilpatrick because those references, even if combined, fail to teach or suggest all the claim

limitations of the claimed invention and, therefore, fail to make a *prima facie* case of obviousness.

Appellant submits that Kilpatrick also fails to teach or suggest the persistent region of volatile memory that is not directly written to by the operating system, as recited in the claimed invention. Kilpatrick teaches a cache control circuit that allows a portion of the cache to be "locked," that is, data values in the "locked" portion of the cache are not replaced when new data is stored in the cache. (See Kilpatrick, Abstract). Kilpatrick does not teach that his disclosed cache memory is not reset during a boot cycle. Nor does Kilpatrick otherwise teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized on a boot cycle.

Williams, Stein and Kilpatrick fail to teach or suggest a computer having a volatile memory separated into a first, contiguous, non-persistent region and a second, contiguous, persistent memory in which the persistent region of volatile memory is not directly written to by the operating system and is not initialized during a boot cycle. Accordingly, Appellant respectfully submits that the combination of Williams, Stein and Kilpatrick does not teach or suggest the invention recited by independent claim 15, that claims 16-17 define patentably over the combination of Williams, Stein and Kilpatrick, and that the rejection of those claims under 35 U.S.C. §103 should be reversed.

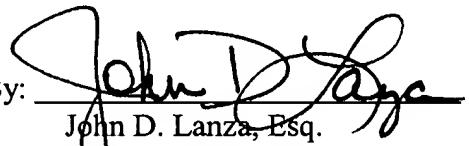
8.5 Claim 12 is improperly objected to because claim 11, which claim 12 depends from, recites patentable subject matter.

Claim 12 is objected to as being dependent on a rejected base claim. Claim 12 depends from independent claim 11. In light of the foregoing arguments, Appellant respectfully submits that claim 11 recites patentable subject matter. Accordingly, it is Appellant's position that the objection to claim 12 is improper and should be withdrawn.

IX. CONCLUSION

In light of the foregoing arguments, Appellant submits that pending claims 1-23 are patentable when compared to the prior art of record and respectfully requests that the Board to reverse the Examiner's final rejection of claims 1-23.

Respectfully submitted,
LAHIVE & COCKFIELD, LLP

By: 
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Dated June 21, 2004

APPENDIX A

1. A computer operating under control of an operating system, the computer comprising:

a volatile memory, including a first, contiguous, non-persistent memory region, the first non-persistent memory region directly accessible by the operating system, and initialized during a boot cycle, and a second contiguous persistent memory region not directly accessible by the operating system and not initialized during a boot cycle; and

an intermediary program in communication with the operating system and the second, persistent memory region,

wherein the intermediary program enables the operating system to address the second, persistent memory region.

2. The computer of claim 1 wherein the first, non-persistent memory region and the second, persistent memory region comprise different physical volatile memory elements.

3. The computer of claim 1 wherein the intermediary program is a device driver.

4. The computer of claim 1 additionally comprising:

a basic input/output system (BIOS) preventing direct access to the second, persistent memory region by the operating system.

5. The computer of claim 1 wherein the second, persistent memory region is allocated to redundant CPU memory locations.

6. The computer of claim 1 additionally comprising:

a non-volatile memory element storing information concerning the configuration of the second, persistent memory region.

7. The computer of claim 1 additionally comprising:

a non-volatile memory, element storing information concerning the configuration of the first, non-persistent memory region.

8. The computer of claim 1 additionally comprising:

a file storing information concerning the configuration of the second, persistent memory region.

9. The computer of claim 1 additionally comprising:

a file storing information concerning the configuration of the first, non-persistent memory region.

10. The computer of claim 1 wherein the persistent memory region comprises:

a look-aside buffer, comprising:

a set of state bits, and

a buffer region for the storage of data,

wherein the look-aside buffer is used for the atomic storage and update of write requests.

11. A storage medium having embodied thereon a program which, when loaded into a computer having an operating system and a volatile memory partitioned into a first, contiguous non-persistent memory region and a second, contiguous, persistent memory region, provides the computer with a persistent, volatile memory, said program comprising:

computer-readable program means for reading from the second, persistent memory region in response to requests coming from the operating system; and

computer-readable program means for writing to the second, persistent memory region in response to requests coming from the operating system.

12. The program of claim 11 wherein the second, persistent memory region of the computer comprises a look-aside buffer including a set of state bits and a buffer region for the storage of data, the program further comprising:

computer-readable program means for setting the state bits to a first value before writing the contents of a request to the buffer region;

computer-readable program means for writing the contents of a request to the buffer region;

computer-readable program means for setting the state bits to a second value after successful completion of the writing of the contents of a request to the buffer region;

computer-readable program means for copying the contents of the buffer region to the appropriate location in the second, persistent memory region; and

(b-e) computer-readable program means for setting the state bits to a third value after successfully copying the contents of the buffer region to the appropriate location in the second, persistent memory region.

13. In a computer system comprising an operating system, an intermediary program, and a volatile memory, a method for providing a persistent region of the volatile memory, the method comprising the steps of:

(a) partitioning the volatile memory into a first, contiguous, non-persistent memory region and a second, contiguous, persistent memory region;

(b) providing an intermediary program in communication with the second, persistent memory region such that the second, persistent memory region is accessible to the operating system solely through the device driver.

14. The method of claim 13 wherein the contents of the second, persistent memory region are not initialized during a boot cycle.

15. The method of claim 13 wherein the second, persistent memory region comprises a look-aside buffer used by the intermediary program for atomic update and storage of write requests.

16. The method of claim 13 wherein step (a) comprises the steps of:

(a-a) reading a stored address defining the start address of the second, persistent memory region;

(a-b) reading a stored value defining the size of the second, persistent memory region; and

(a-c) creating a second, persistent memory region at the start address equal in size to the stored value defining the size of the second, persistent memory region.

17. The method of claim 16 wherein the program reads the stored addresses and stored values defining the size of the second, persistent memory region from a non-volatile memory element.

18. An operating system memory environment comprising:

a first, contiguous memory mode region of volatile memory accessible to users and to the operating system;

a second, contiguous memory mode region of volatile memory accessible only to the operating system and not to users; and

a third, contiguous memory mode region of volatile memory not accessible by users and not directly accessible by the operating system.

19. The operating system memory environment of claim 18 wherein the operating system is a Microsoft Windows operating system.

20. A computer operating under control of a memory-mapped operating system, the computer comprising:

a volatile memory including a first, contiguous, non-persistent memory region that is mapped by the operating system; and

a second, contiguous, persistent memory region that is not mapped by the operating system.

21. The computer of claim 20 further comprising:

a device driver in communication with the operating system and the second, persistent region of volatile memory,

wherein the operating system addresses the second, persistent region of volatile memory using the device driver.

22. The computer of claim 21 wherein the second, persistent region of volatile memory comprises a look-aside buffer used by the device driver for atomic update and storage of write requests.

23. The computer of claim 20 wherein the locations of the second, persistent region of volatile memory are mapped by the operating system or a user application upon completion of the boot cycle.